

What is claimed is:

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1. A method for processing instructions in a superscaler microprocessor, comprising:
- 2 selecting an initial sequence of instructions for inclusion in a trace cache line;
- 3 determining a set of rename resources needed for said trace cache line on a per-
- 4 packet basis;
- 5 adding one or more provisional instructions to said trace cache line to create a
- 6 provisional trace cache line;
- 7 repeating said determining step for said provisional trace cache line;
- 8 comparing said set of rename resources needed for said provisional trace cache
- 9 line to a rename capacity; and
- 10 accepting said one or more provisional instructions for inclusion in said trace line
- 11 and repeating said adding step, or rejecting said one or more provisional instructions,
- 12 based on said comparing step.
- 1 2. A method in accordance with claim 1, wherein:
- 2 said set of rename resources needed and said rename capacity include a source
- 3 parameter.
- 1 3. A method in accordance with claim 1, wherein:
- 2 said set of rename resources needed and said rename capacity include a destination
- 3 parameter.

1 4. A method in accordance with claim 1, wherein:

2 said set of rename resources needed and said rename capacity include a line size
3 parameter.

1 5. A method in accordance with claim 1, wherein:

2 determining a set of rename resources needed on a per-packet basis excludes
3 destinations subsequently over-written within the packet from said set of rename
4 resources needed.

1 6. A method in accordance with claim 1, wherein:

2 determining a set of rename resources needed on a per-packet basis excludes
3 redundant sources within the packet from said set of rename resources needed.

1 7. A method in accordance with claim 1, wherein:

2 determining a set of rename resources needed on a per-packet basis excludes
3 sources created within said trace cache line.

1 8. A method in accordance with claim 1, wherein:

2 selecting said initial sequence of instructions uses a worst case assumption of said
3 set of rename resources needed.

AI 1 9. A method in accordance with claim 1, wherein:

2 selecting said initial sequence of instructions includes tabulating a maximum rename
3 resource cumulative total based on a plurality of instruction types.

1 10. A method in accordance with claim 1, wherein:

2 selecting a number of provisional instructions is performed based on a difference
3 between said set of rename resources needed and said rename capacity.

1 11. An apparatus for processing instructions in a superscale microprocessor,
2 comprising:

3 an instruction stream with a plurality of instructions;
4 a trace cache line for receiving said instructions from said instructions stream;
5 a packetized instruction resource calculator for determining a set of rename
6 resources needed for said instructions in said trace cache line;
7 an instruction adder, responsive to said packetized instruction resource calculator,
8 for adding one or more instructions to said trace cache line from said instruction stream
9 while said set of rename resources needed is less than a rename resource capacity.

1 12. An apparatus in accordance with claim 11, wherein:

2 said set of rename resources needed includes a source parameter.

1 13. An apparatus in accordance with claim 11, wherein:
2 said set of rename resources needed included a destination parameter.

1 14. An apparatus in accordance with claim 11, wherein:
2 said set of rename resources needed includes a line size parameter.

1 15. An apparatus in accordance with claim 14, wherein:
2 said set of rename resources needed includes a source parameter.

1 16. An apparatus in accordance with claim 15, wherein:
2 said set of rename resources needed includes a destination parameter.

1 17. An apparatus in accordance with claim 11, wherein:
2 said packetized instruction resource calculator excludes destinations subsequently
3 over-written within said trace cache line from said set of resources needed.

1 18. An apparatus in accordance with claim 17, wherein:
2 said packetized instruction resource calculator excludes redundant sources with
3 said trace cache line from said set of resources needed.

1 19. An apparatus in accordance with claim 18, wherein:

AI 2 said packetized instruction resource calculator excludes sources created within
3 said trace cache line.

1 20. An apparatus in accordance with claim 11, further comprising:

2 a trace cache line initializer for initially loading said trace cache line with an initial
3 number of instructions.

1 21. An apparatus in accordance with claim 20, wherein:

2 said initial number of instructions is calculated as a fraction of said rename
3 resource capacity.

1 22. A method of creating cache lines of instructions in a computer system,

2 comprising:

3 determining the number of instructions in the cache lines using a packetization of
4 instructions technique and a dynamic cache line size;

5 matching said dynamic cache line size to a rename unit capacity.

1 23. A method in accordance with claim 22, wherein:

2 matching said dynamic cache line size includes eliminating redundant register
3 references within the cache lines.